WHAT IS CLAIMED IS

1. A semiconductor memory device, comprising:

a plurality of bit line pairs, each of which includes a first bit line and a second bit line;

a plurality of memory cells which are coupled to said first bit line, and store electric charge in capacitors;

a dummy cell which is coupled to a second bit line, and is charged with a predetermined potential;

a sense amplifier which amplifies a potential difference between the first bit line and the second bit line; and

a control circuit which charges said dummy cell with the predetermined potential only for a fixed time period.

2. The semiconductor memory device as claimed in claim 1, wherein said fixed time period is constant regardless of intervals at which access is made to said bit line pairs.

3. The semiconductor memory device as claimed in claim 2, further comprising:

a first timer circuit which generates an

instruction signal at first predetermined intervals to order charging of said dummy cell with the predetermined potential; and

a first address generating circuit which generates an address in response to the instruction signal from said first timer circuit,

wherein said control circuit charges said dummy cell corresponding to said address with the predetermined potential in response to the instruction signal.

4. The semiconductor memory device as claimed in claim 3, wherein said control circuit immediately charges, in response to the instruction signal, said dummy cell corresponding to said address with the predetermined potential when said first timer circuit generates the instruction signal while said bit line pairs are not being accessed, and wherein said control circuit charges said dummy cell corresponding to said address with the predetermined potential after an end of access when said first timer circuit generates the instruction signal while said bit line pairs are being accessed.

5. The semiconductor memory device as claimed in claim 3, further comprising:

a second timer circuit which generates an instruction signal at second predetermined intervals to order refreshing of said memory cells; and

a second address generating circuit which generates an address of memory cells to be refreshed

in response to the instruction signal from said second timer circuit.

6. The semiconductor memory device as claimed in claim 3, wherein said first timer circuit generates a refresh instruction signal at second predetermined intervals to order refreshing of said memory cells, said semiconductor memory device further comprising an address generating circuit which generates an address of memory cells to be refreshed in response to the refresh instruction signal from said first timer circuit.

7. The semiconductor memory device as claimed in claim 3, wherein said control circuit refreshes the memory cells at said address in addition to charging the dummy cell corresponding to said address with the predetermined potential in response to the instruction signal generated by said first timer circuit.

8. The semiconductor memory device as claimed in claim 7, wherein said bit line pairs are divided into a plurality of blocks, and said first address generating circuit generates successive addresses first for all word addresses in a given one of the blocks and then for a next one of the blocks.

9. The semiconductor memory device as claimed in claim 7, wherein said bit line pairs are divided into a plurality of blocks, and said first address generating circuit generates successive addresses first for a given word address in all the blocks and then for a next word address.